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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,077	09/19/2003	Douglas R. Moran	42P17504	8441

7590 10/27/2008
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EXAMINER

GELAGAY, SHEWAYE

ART UNIT	PAPER NUMBER
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2437

MAIL DATE	DELIVERY MODE
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10/27/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/666,077	Applicant(s) MORAN ET AL.	
	Examiner SHEWAYE GELAGAY	Art Unit 2437	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 12-20 is/are pending in the application.
- 4a) Of the above claim(s) 7-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 12-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/16/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Claims 7-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on July 10, 2008.
2. Claims 1-6 and 12-20 have been examined.

Drawings

3. Figures 1 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2137

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Own Admitted Art (hereinafter Admission) in view of Koo US 5,155,829.

As per claim 1:

Admission discloses a prioritized address decoder comprising: a first comparator to compare a destination device address of data with a first address range associated with a first device; (figure 2, page 1, pp. 4-6) and a second comparator coupled to the first comparator to compare the destination device address with a second address range associated with a second device, wherein the data is sent to the second device in response to a first output of the first comparator and a second output of the second comparator. (figure 2, page 1, pp. 4-6)

Admission does not explicitly disclose data is sent to the second device in response to a first output of the first comparator. Koo in analogous art, however, discloses that data is sent to the second device in response to a first output of the first comparator. (figure 3, col. 5, lines 42-67) Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the system disclosed by Admission with Koo in order to provide a secure memory system in which attempts to improperly access the programs stored in the system are detected and an appropriate action to counter the attempt is made. (col. 2, lines 6-9; Koo)

As per claims 2 and 4:

The combination of Admission and Koo teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the first comparator disables the second comparator when the destination device address is within the first

Art Unit: 2137

address range. (figure 3, col. 5, lines 42-67)

As per claim 3:

The combination of Admission and Koo teaches all the subject matter as discussed above. In addition, Admission further discloses an address decoder that includes a number of comparators connected in parallel. Each comparator compares the destination address of the data with an address range of a device within the system. In addition, Koo further an address block A which is stored in address comparator 34, address comparator 36 monitors one or more addresses in code block B, the address block A which is stored in address comparator 34 is applied to comparator 34 will produce a logical 1 signal ...at such time comparator 36 detects the address in block B that is stored in it, the comparator 36 will produce a logical 1. Both references do not explicitly disclose wherein the data is sent to the third device in response to a third output of the third comparator, the second output of the second comparator, and the first output of the first comparator. It would have been obvious to one ordinary skill in the art to include a second output of the second comparator in Koo in the third comparator coupled to the first and second comparator to compare destination device address with a third device disclosed in Admission to achieve the claimed invention. As disclosed in Koo the combination would be to in order to provide secure memory system in which attempts to improperly access the programs stored in the system are detected. col. 2, lines 6-9; Koo)

As per claim 5:

The combination of Admission and Koo teaches all the subject matter as discussed above. In addition, Admission further discloses wherein the first address range is associated with a first device of a computer system, secured data in the computer system is authorized to be sent to the first device. (figure 2, page 1, pp. 4-6)

As per claim 6:

The combination of Admission and Koo teaches all the subject matter as discussed above. In addition, Admission further discloses wherein the second address range is associated with a second device of the computer system, the secured data is not authorized to be sent to the second device. (figure 2, page 1, pp. 4-6)

6. Claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Own Admitted Art (hereinafter Admission) in view of Koo US 5,155,829 and in view of Yamazaki et al. (hereinafter Yamazaki) US 5,940,342.

As per claim 12:

Admission discloses a computer system comprising: a memory controller comprising a prioritized address decoder, the prioritized address decoder including a first comparator to compare a destination device address of data with a first address range associated with a first device; (figure 2, page 1, pp. 4-6) and a second comparator coupled to the first comparator to compare the destination device address with a second address range associated with a second device, wherein the data is sent to the second device in response to a first output of the first comparator and a second output of the second comparator. (figure 2, page 1, pp. 4-6)

Admission does not explicitly disclose data is sent to the second device in response to a first output of the first comparator. Koo in analogous art, however, discloses that data is sent to the second device in response to a first output of the first comparator. (figure 3, col. 5, lines 42-67) Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the system disclosed by Admission with Koo in order to provide a secure memory system in which attempts to improperly access the programs stored in the system are detected and an appropriate action to counter the attempt is made. (col. 2, lines 6-9; Koo)

Both references do not explicitly disclose a dynamic random access memory (DRAM); and a memory controller, coupled to the DRAM. Yamazaki in analogous art, however discloses a dynamic random access memory (DRAM); and a memory controller, coupled to the DRAM. Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the system disclosed by Admission and Koo with Yamazaki in order to provide a memory device which can access necessary data at high speed, and a control circuit therefor. (col. 6, lines 12-13; Yamazaki)

As per claim 13:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the first comparator disables the second comparator when the destination device address is within the first address range. (figure 3, col. 5, lines 42-67)

As per claim 14:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Admission further discloses an address decoder that includes a number of comparators connected in parallel. Each comparator compares the destination address of the data with an address range of a device within the system. In addition, Koo further an address block A which is stored in address comparator 34, address comparator 36 monitors one or more addresses in code block B, the address block A which is stored in address comparator 34 is applied to comparator 34 will produce a logical 1 signal ...at such time comparator 36 detects the address in block B that is stored in it, the comparator 36 will produce a logical 1. Both references do not explicitly disclose wherein the data is sent to the third device in response to a third output of the third comparator, the second output of the second comparator, and the first output of the first comparator. It would have been obvious to one ordinary skill in the art to include a second output of the second comparator in Koo in the third comparator coupled to the first and second comparator to compare destination device address with a third device disclosed in Admission to achieve the claimed invention. As disclosed in Koo the combination would be to in order to provide secure memory system in which attempts to improperly access the programs stored in the system are detected. col. 2, lines 6-9; Koo)

As per claim 15:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the first address range is

associated with a trusted agent. (figure 3, col. 5, lines 42-67)

As per claim 16:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses a processor coupled to the memory controller, wherein the trusted agent is the processor. (figure 3, col. 5, lines 42-67)

As per claim 17:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the second address range is associated with a non-trusted agent. (figure 3, col. 5, lines 42-67)

As per claim 18:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the memory controller further comprises a plurality of configuration registers storing information on the first and the second address ranges. (figure 3, col. 5, lines 42-67)

As per claim 19:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the information is stored in the plurality of configuration registers during configuration. (figure 3, col. 5, lines 42-67)

As per claim 20:

The combination of Admission, Koo and Yamazaki teaches all the subject matter as discussed above. In addition, Koo further discloses wherein the plurality of configuration registers are locked during a trusted mode. (figure 3, col. 5, lines 42-67) Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHEWAYE GELAGAY whose telephone number is (571)272-4219. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 571-272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. G./
Examiner, Art Unit 2437

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2437

Application/Control Number: 10/666,077
Art Unit: 2137

Page 10